# Single-Crystal $C_{60}$ Needle/CuPc Nanoparticle Double Floating-Gate for Low-Voltage Organic Transistors Based Non-Volatile Memory Devices

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Field-effect transistor (FET)-type memory devices have been widely investigated recently because of their non-destructive read-out property, single transistor realization, and excellent compatibility with complementary metal oxide semiconductor (CMOS) devices.[1–9] Among them, floating-gate memory based on a FET structure has an electrically isolated conducting gate,[10] which can be used as charge storage sites for charging or discharging during the programming and erasing processes. Precise control of the amount of charge stored in the specific floating-gate to set the bits of a memory cell could solve the fundamental scaling-down problem and meet the requirement for high-density memory devices.[3,5,11–13] Therefore, a discrete floating-gate utilizing nanostructured materials rather than a conventional planar floating-gate can determine the size and density of charge-trapping elements in a uniform distribution for future superior high-density memory. The following possibilities have already been employed to fashion nanostructured floating-gate devices:[12,13] i) thermal evaporation of thin metal layers or metal islands (nanoparticles (NPs));[1,14–18] ii) chemisorbed or electrostatic self-assembled metal monolayers;[19–24] iii) block polymer/NP composites;[25–27] iv) carbon-based charge trapping materials, such as $C_{60}$ or graphene.[28–33] However, the above floating-gate-based memory devices generally utilize a single floating-gate that stores only one kind of charge (hole or electron) to signify a "1" or "0" digital state as one bit of information.[3,5] To meet the future demand for product miniaturization and high density, memory properties such as memory window, retention, endurance, and integration still need to be enhanced. If two floating-gates were assembled in one device, the memory device could potentially store data at higher density in the same physical space during the non-volatile mode and also suppress leakage of the stored charge as a result of the band offset or Coulomb repulsion between the upper and lower floating-gates.[24,34–36] On the other hand, memories that allow the coexistence of trapping charges in both polarities (ambipolar trapping) result in a large bi-directional threshold voltage shift and correspondingly large memory window for designing multi-level flash memory.[23,37,38] However, optimizing the memory materials and structures to enable continuous scaling has remained a significant challenge until now. In particular, the detailed mechanism and design principles for organic non-volatile memory with a double floating-gate are not clear.

In the work reported here, we first compatibly combined the three concepts of "double floating-gate",[24,34–36,39,40] "ambipolar charge carrier trapping",[23,37,38] and "discrete trapping sites"[12,13] to produce high-performance non-volatile charge-trapping memory based on organic FET (OFET) device structures. Such heterostructure double floating-gate memory devices achieved a large charge storage capacity and a high density of available independent trapping sites that enable stable operation by displaying long retention. **Figure 1** shows a schematic diagram of prototype pentacene-based OFET memories on an indium tin oxide (ITO) glass substrate with a bottom-gate top-contact (BGTC) structure using radio-requency (RF)-sputtered high dielectric constant (high $k$) $HfO_2$ as an insulating dielectric. The double floating-gate device structure was formed from the semiconducting channel and heterostructured dual chargeable layers of copper phthalocyanine (CuPc) NPs/single-crystal fullerene ($C_{60}$) needles (N-$C_{60}$) covered by a crosslinked poly(4-vinylphenol) (c-PVP) tunneling barrier. Discrete p-type CuPc NPs and n-type N-$C_{60}$ were independently selected as the hole and electron trapping sites for the above double floating-gate transistor memory to further enhance memory window and related data storage capacity. N-$C_{60}$ trapping sites (diameters ca. 590 ± 15 nm) were first fabricated, and then thermally evaporated CuPc NPs (ca. 15 ± 3 nm) were deposited discretely on the N-$C_{60}$ or the $HfO_2$ interface. The OFET memories were characterized by the gate response at room temperature in a $N_2$-filled glove box to eliminate atmospheric moisture. In a systematic investigation, memory characteristics of double floating-gate devices were impartially compared to those of individual single floating-gate memory structures (N-$C_{60}$- or CuPc-only devices).

N-$C_{60}$ as a discrete floating-gate was synthesized by a droplet crystallization method[41] with evaporation of the drop-coating $C_{60}$ solution in $m$-xylene on the $HfO_2$/ITO glass substrate. A representative morphological study of N-$C_{60}$ based on the optical-microscopy and transmission electron microscopy (TEM) images is presented in Figure S1 in the Supporting Information. The as-grown N-$C_{60}$ crystals are needle shaped with effective aspect ratios (the ratio of the needle length to the diameter) of 5, 7, 17, and 45, prepared from solutions with concentrations of 0.01, 0.05, 0.1, and 1 mg $mL^{-1}$, respectively. Note that the abbreviation N-$C_{60}$-X means needle-shaped $C_{60}$ single

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DOI: 10.1002/adma.201403771

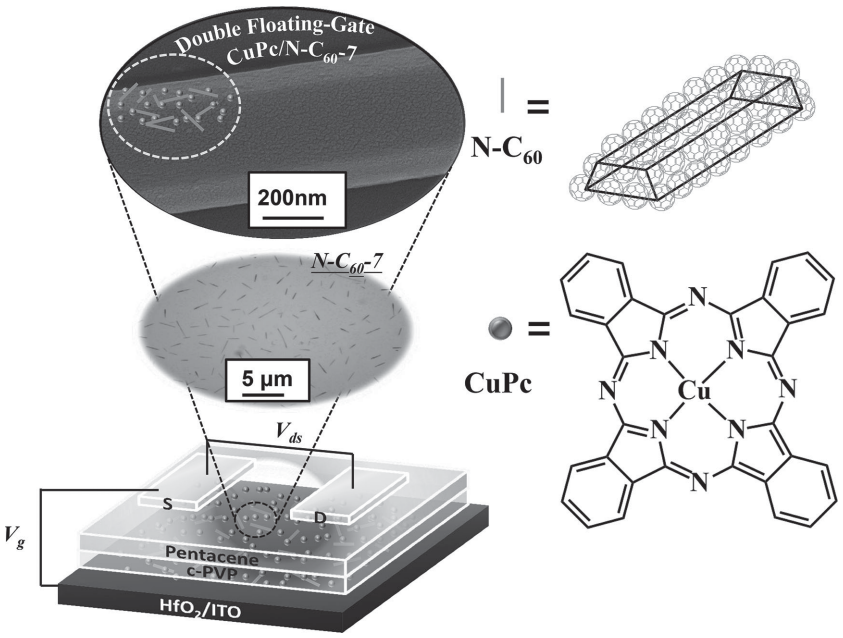


**Figure 1.** Schematic cross-sectional diagram of the pentacene-based OFET memory device with the CuPc/N-$C_{60}$ double floating-gate, along with optical microscopy and TEM images.

crystals with aspect ratio X. The well-dispersed needle-shaped crystals of N-$C_{60}$-7 shown in Figure 1 have diameters of a few hundred nanometers with a hexagonal structure, similar to that reported in the literature.[41] They are without significant physical contact between individual $C_{60}$ needles and such well-separated N-$C_{60}$ crystals with a high density could be beneficial for realizing a floating-gate non-volatile memory with improved charge storage properties.[42] However, as the $C_{60}$ needles grow (for the case of N-$C_{60}$-17 and N-$C_{60}$-45), the $C_{60}$ needles can freely cross over each other, as observed experimentally in Figure S1 in the Supporting Information.

To confirm that the memory effect originated from the presence of "ambipolar charge trapping" based on hole trapping in CuPc and electron trapping in N-$C_{60}$-7, a charging $V_g$ of −5 V/+5 V with a fixed $V_d$ of −5 V was applied as a pulse stimulus with a duration of 1 ms, as shown in **Figure 2**a for a N-$C_{60}$-7/CuPc double floating-gate device and Figures 2b and c for CuPc and N-$C_{60}$-7 individual single floating-gate devices, respectively. First, the CuPc-only device (Figure 2b) exhibits the first initial (I) curve and almost no significant change (second curve) as the programming ($P^e$) voltage pulse (5 V) is applied. This means that the electrons cannot be trapped in the CuPc trapping element. During the erasing operation (a $V_g$ pulse of −5 V; $E^h$ process), the holes accumulated in the channel are injected into the CuPc NPs. Note that the superscripts "h" and "e" mean the programming (P)/erasing (E) processes involving holes and electrons, respectively. A certain number of charging holes, stored in the CuPc floating-gate, induces a built-in field opposite to the applied $V_g$, which results in a parallel shift of the transfer curve in the negative direction ($E^h$ process). Furthermore, during the subsequent programming ($P^h$) operation by a $V_g$ pulse of 5 V, the transfer curve shifts in the positive direction and returns to the position of the initial state, indicating that the holes stored in the CuPc come back to the channel. A memory window of ca. 1.4 V between the erased ($E^h$) and initial (I) states obtained for CuPc NP floating-gate memory devices results from the altered charge distribution in the OFET, which arises from the positive charge trapping/detrapping process in CuPc NPs. Correspondingly, a significant shift in threshold voltage of 3.2 V in the N-$C_{60}$-7 floating-gate device is observed only after an appropriate programming ($P^e$) voltage of 5 V is applied (Figure 2c); that is, the application of a positive voltage pulse results in only electron carriers being transferred to the N-$C_{60}$-7 trapping component. The trapped electrons partially strengthen the external applied electric field and result in a high conductance state and an associated positive threshold voltage shift. Clearly, unipolar trapping results in threshold voltage shifts only in one direction and the memory behavior here is achieved by trapping and releasing holes and electrons in the individual CuPc NPs and N-$C_{60}$-7 single floating-gate memory, respectively.

However, from the p-type channel (hole enhancement mode) in the heterostructure N-$C_{60}$-7/CuPc double floating-gate combined memory, the threshold voltage shifts to the positive direction relative to the initial (I) state after the positive gate bias (programming process, $P^e$), as shown in Figure 2a. It also shifts to the negative direction from the

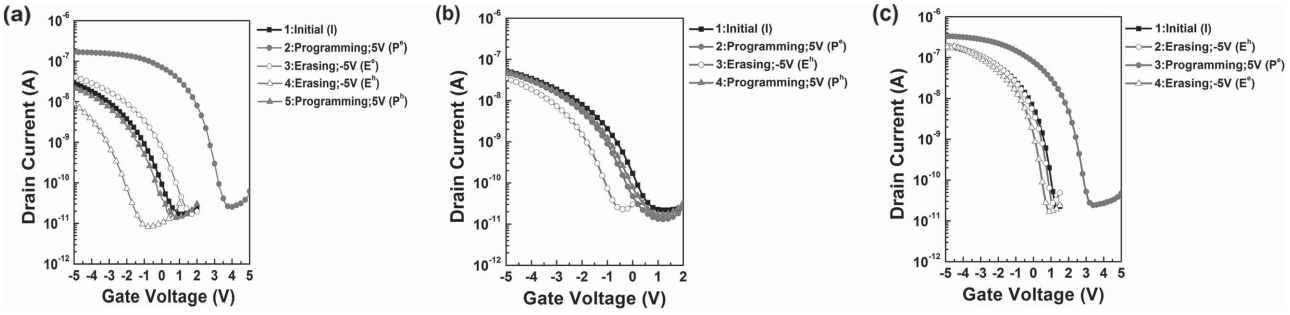


**Figure 2.** Transfer characteristics of: a) CuPc/N-$C_{60}$-7 double floating-gate and b) CuPc and c) N-$C_{60}$-7 single floating-gate memories under programming/erasing operation.

$E^e$ scan (same position as the initial curve) after a further applied negation gate bias (erasing process, $E^h$). Here, the threshold voltages for the p-type channel of the floating-gate memory after $P^e$ and $E^h$ are 3.1 and −1.3 V, respectively, which represent negative and positive charges trapped on the electron-rich N-$C_{60}$-7 and hole-rich CuPc NPs, respectively. However, during the $E^e$ and $P^h$ operations, some trapped charges are discharged or the charges with opposite polarities tunnel into the trapping site to electrically balance the residual trapping charges, and then the device returns to the initial state (I). As a result, a conspicuous memory window of 4.4 V is obtained between two states after the $P^e$ and $E^h$ processes. This indicates the formation of a N-$C_{60}$-7/CuPc double floating-gate memory device with a broadened memory window due to the independent trapping of both electrons and holes (ambipolar trapping). Therefore, the strategies for ambipolar trapping through additional heterostructured double floating-gate layers could achieve a larger memory window than the unipolar trapping counterpart with single floating-gate layers.

Counterclockwise hysteresis in the transfer curve of the CuPc/N-$C_{60}$-7 double floating-gate memory device under different gate sweeping voltages further confirms the ambipolar charge trapping behavior (**Figure 3**a,b). The apparent memory window should be crucially illustrated by the overall charge balance between the channel, floating-gate, and applied control gate bias. The change in threshold voltage of the double floating-gate memory device is progressively more significant towards the negative/positive direction obtained in the backward/forward sweeping process of Figure 3a/Figure 3b as increasing sweeping (erasing/programming) gate voltages to more negative/positive values can be understood in terms of the hole/electron trapping effect. Here, it is clear that the double floating-gate memory device has the potential ability to systematically trap both electrons and holes, in good agreement with the results shown in Figure 2a. Besides, threshold voltage can be shifted towards a more positive $V_g$ compared with a negative $V_g$ during the same dual sweep range (2 V to −5 V vs. 5 V to −2 V), which is thought to clarify that the higher electric field generated in the confined dimension of the $C_{60}$ needle facilitates the formation of the dipole orientation that stabilizes the electron trapping condition. It also conclusively proves that holes/electrons trapped in individual CuPc/N-$C_{60}$-7 can avoid double floating-gate coupling interference.

Figure 3c shows the transfer characteristics ($I_d^{1/2}$ versus $V_g$) of single and double floating-gate memory devices during dual sweeping within the range from 5 V to −5 V. The charge flow at the pentacene-channel/floating-gate interface can be regulated by applying the gate voltage field. All the OFETs exhibit p-type characteristics, and a remarkably counterclockwise hysteresis window of 4.2 V is evident for the CuPc/N-$C_{60}$-7 double floating-gate device (orange line; square symbols) while CuPc (pink line; triangles) and N-$C_{60}$-7 (blue line; circles) single floating-gate devices have memory windows of 0.6 and 3.1 V, respectively. During the negative sweep (from 5 V to −5 V), the device turns ON and then there is a rapid increase in $I_d$ with a negative $V_g$ owing to the absence of the trapping charges or discharged floating-gate. As $V_g$ approaches zero, $I_d$ still remains in the high conductance state with non-volatile character. Then, a voltage shift to the left and a decrease in $I_d$ during the subsequent sweep in the positive direction (reverse voltage sweep; from −5 to 5 V) are shown. This suggests that the charge on the floating-gate screens the applied electric field, which is manifested as a more negative voltage needed to induce accumulation on the pentacene channel. Besides, the non-volatility based on the trapping charge keeps the device in the low conductance state. Note that the transfer curves in the forward and reverse sweeps of the CuPc/N-$C_{60}$-7 double floating-gate memory device overlap that in the forward sweep of N-$C_{60}$-7 and the reverse sweep of CuPc single floating-gate devices, respectively. This suggests that the initial 5 V gate bias charges the floating-gate negatively, contributed from N-$C_{60}$-7, resulting in a programming state (same operation as $P^e$ in Figure 2a). Relatively,

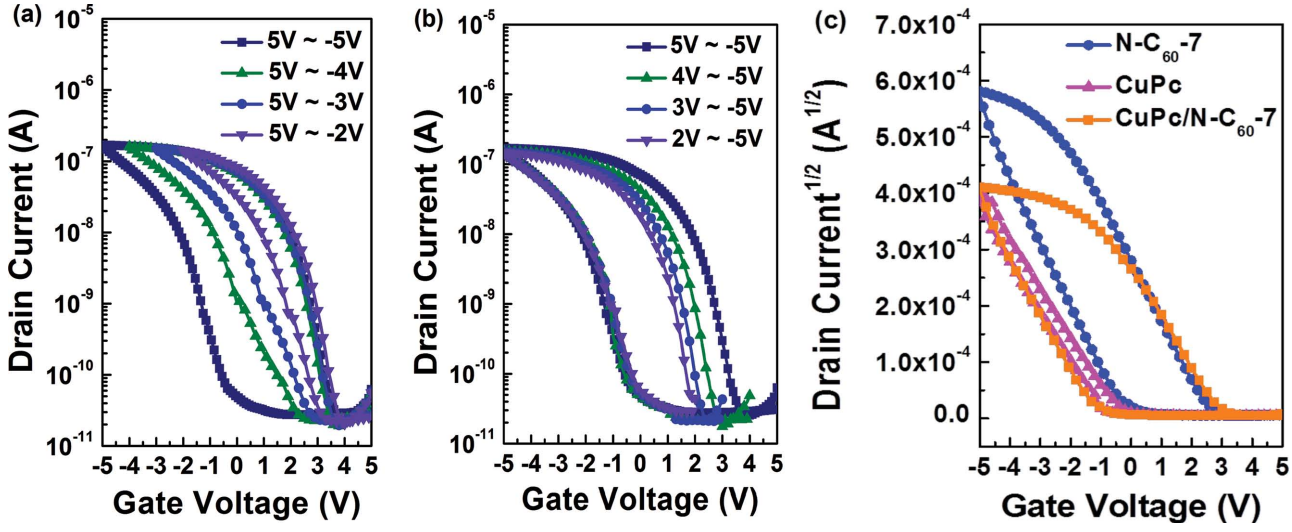


**Figure 3.** Transfer characteristics of CuPc/N-$C_{60}$-7 double floating-gate memory with gate voltage scanned a) from 5 V to various negative gate voltages and b) from various positive gate voltages to −5 V. c) Transfer characteristics of N-$C_{60}$-7 and CuPc single floating-gate and CuPc/N-$C_{60}$-7 double floating-gate memory under dual sweeping scan.

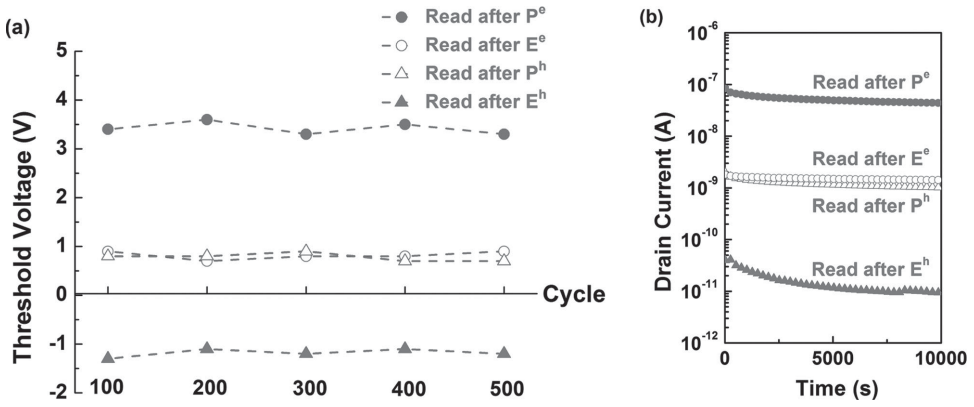


**Figure 4.** Endurance test (a) and retention properties (b) of the device monitored after programming ($P^e$), erasing ($E^e$), erasing ($E^h$) and programming ($P^h$) processes.

the erased state is expected to be positive charge being trapped on CuPc NPs in the reverse sweep (same operation as $E^h$ in Figure 2a). When both charge carriers are trapped, the transfer curve extending on both sides contributes to a significantly large threshold voltage shift. The above result suggests that the ambipolar trapping in CuPc/N-$C_{60}$-7 double floating-gate memory is an attractive option for future non-volatile memory with a massive memory capacity.

**Figure 4**a shows the endurance characteristics under repeated programming/erasing cycles of the double floating-gate device, up to 500 cycles. The pulse bias sequence used is programming ($P^e$)/erasing ($E^e$)/erasing ($E^h$)/programming ($P^h$) with four corresponding reading $I_d$–$V_g$ sweeps in every 100 cycles (detailed sweeps in Figure S2 in the Supporting Information). The endurance is consecutively achieved through the application of the control gate voltage pulses (5 V or −5 V) with a duration of 2 s. For the 500 performed endurance cycles, the device maintained stable operation with threshold voltages of 3.4 ± 0.2 V, 0.8 ± 0.2 V, and −1.2 ± 0.1 V for the programming ($P^e$), erasing ($E^e$) (or programming ($P^h$)), and erasing ($E^h$) states, respectively, even though there is a slight fluctuation. It is believed that all the observed endurance fluctuations are from measurement disturbance (experimental errors) rather than interface degradation. When the threshold voltage is moved from positive to negative or from negative to positive with respect to the gate pulse, the trapped holes or electrons can be measured independently and the net memory window increases by the discrete dual-channel chargeable storage node. Besides, the stability of the four states ($P^e$, $E^e$, $E^h$, and $P^h$) is further monitored by the time-resolved behavior at a constant $V_d$ of −5 V (Figure 4b). During the first 200 s, there is a slight degradation in current of all the programming/erasing states and then the memory window defined by the difference between the $P^e$ (enriched with electrons) and $E^h$ (enriched with electrons) states is retained at a constant value of 3–4 orders of magnitude for up to $10^4$ s. The observed $E^e$ and $P^h$ states with a similar current level of ca. $10^{-9}$ A indicate that the corresponding electrical operation can recover, i.e., return to the initial (I) state in the discharged condition. The prepared heterostructure N-$C_{60}$/CuPc double floating-gate show an excellent retention for non-volatile organic memory, and leakage can be negligible if a thick-enough c-PVP layer insulates the charge relaxation. Note that the heterostructure N-$C_{60}$/CuPc double floating-gate memory can be used to read at least three distinct signals (at $P^e$, $E^e$ (or $P^h$), and $E^h$ states). The tri-stable conductance states are capable of storing more than a single bit of information, leading to a multi-level memory cell with an exponential increase in data storage capacity.

Various OFET memory device characteristics of devices using the N-$C_{60}$ and CuPc NP single floating-gate and heterostructure CuPc/N-$C_{60}$ double floating-gate are listed in **Table 1**, including the saturated mobility ($\mu$), ON/OFF ratio ($I_{on}/I_{off}$),

**Table 1.** OFET memory device characteristics using various floating-gates.

| Floating-gate | Mobility [$cm^2 V^{-1} s^{-1}$] | ON/OFF ratio | Memory window [V] | Stored electron density [charges per needle] | Stored hole density [charges per NP] |
|---|---|---|---|---|---|
| N-$C_{60}$-5 | $2.81 \times 10^{-2}$ | $1.1 \times 10^3$ | 1.2 | 309 | – |
| N-$C_{60}$-7 | $3.13 \times 10^{-2}$ | $1.8 \times 10^4$ | 3.2 | 818 | – |
| N-$C_{60}$-17 | $4.53 \times 10^{-2}$ | $5.1 \times 10^2$ | 0.7 | 177 | – |
| N-$C_{60}$-45 | $6.24 \times 10^{-2}$ | $2.4 \times 10^2$ | 0.5 | 131 | – |
| $C_{60}$[a)] | $1.28 \times 10^{-2}$ | $5.9 \times 10^3$ | 0 | – | – |
| CuPc | $6.28 \times 10^{-2}$ | $5.4 \times 10^3$ | 1.4 | – | 67 |
| N-$C_{60}$-7/CuPc | $1.25 \times 10^{-2}$ | $8.3 \times 10^3$ | 4.4 | 727 | 57 |

[a)] $C_{60}$:c-PVP blend as floating-gate.

and memory window ($\Delta V_{th}$). The corresponding hysteresis in the transfer characteristics of N-$C_{60}$ with different aspect ratios as single floating-gate devices is shown in Figure S3 in the Supporting Information. The enhanced mobility with increasing aspect ratio of N-$C_{60}$ is attributed to the accumulation of the induced hole channel in the pentacene/dielectric layer from the opposite charges based on electron-rich N-$C_{60}$ as the controlling gate bias is applied. This indicates combined effects from the N-$C_{60}$ morphology and the charge transfer at the p/n heterojunction interface.[43,44] On the other hand, N-$C_{60}$ with a high concentration (for example, N-$C_{60}$-17 and N-$C_{60}$-45 devices) leads to an obvious increase in the leakage current (in other words, decrease in ON/OFF ratio) owing to the dense/cross distributed N-$C_{60}$, which reduces the activation energy for the hopping transport process of the charge carriers. The memory window is significantly upgraded by the charge traps on going from the N-$C_{60}$-5 (1.1 V) to the N-$C_{60}$-7 devices (3 V), followed by a small hysteresis for the N-$C_{60}$-17 and N-$C_{60}$-45 (less than 1 V) devices. The intersection of $C_{60}$ crystals based on the high-density N-$C_{60}$-17 and N-$C_{60}$-45 devices gives rise to a rapid dissipation of stored charge through the leakage channel and reduces the charge trapping ability.[18] Under these conditions, charges in the N-$C_{60}$ covered by c-PVP cannot effectively prohibit the charge transport between N-$C_{60}$ by means of the leakage path. However, the device with the isolated and uniformly distributed N-$C_{60}$-7 crystals as the floating-gate exhibits the widest memory window since the discrete available trapping sites can be modulated for device miniaturization and improve the electric field from the shape effect.[33] Subsequently, the structural effect on the charge trapping capacity was quantified by comparing the device with the pure c-PVP layer and direct blending of spherical $C_{60}$:c-PVP in similar concentration (Figure S4 in the Supporting Information). No hysteresis is present for these two devices and thus the shape and electrical properties of $C_{60}$ play an important contribution to the charge trapping memory characteristics as a result of the quantum confinement effect.[21] Hence, the charge storage in the floating-gate can be efficiently modulated by changing the size, density, and shape of n-type $C_{60}$.

OFET memories exhibit saturated field-effect mobilities of $(1.25 \pm 0.35) \times 10^{-2}$, $(3.13 \pm 0.29) \times 10^{-2}$, and $(6.28 \pm 0.24) \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ for CuPc/N-$C_{60}$-7 double floating-gate, N-$C_{60}$-7 single , and CuPc single floating-gate devices, respectively, at $V_d = -5$ V with an ON/OFF ratio >$10^3$, as summarized in Table 1. Besides, the calculated p-channel mobilities in the present OFET memories are independent of the programming/erasing operation. The OFET devices behave as electrical memories after the application of programming ($P^e$)/erasing ($E^h$) $V_g$ of ±5 V, and at $V_g = 0$ V the current in between these two states differs by more than three orders of magnitude (memory ratio > $10^3$) for the double floating-gate memory. As noted, memory windows after the application of programming ($P^e$)/erasing ($E^h$) pulses, obtained from Figure 2, are approximately 4.4 ± 0.2, 3.2 ± 0.8, and 1.4 ± 0.5 V for the devices based on N-$C_{60}$-7/CuPc, N-$C_{60}$-7, and CuPc, respectively. They correspond to the calculated numbers of trapped electrons ($\Delta n^e$) of $1.6 \times 10^{12}$ and $1.8 \times 10^{12}$ cm$^{-2}$ within CuPc/N-$C_{60}$-7 and N-$C_{60}$-7 embedded in the c-PVP, respectively, i.e., about 727 and 818 average charging electrons per $C_{60}$ needle, whereas the numbers of trapped holes ($\Delta n^h$) are $6.8 \times 10^{11}$ and $8.0 \times 10^{11}$ cm$^{-2}$ within N-$C_{60}$-7/CuPc and CuPc, respectively, that is, averages

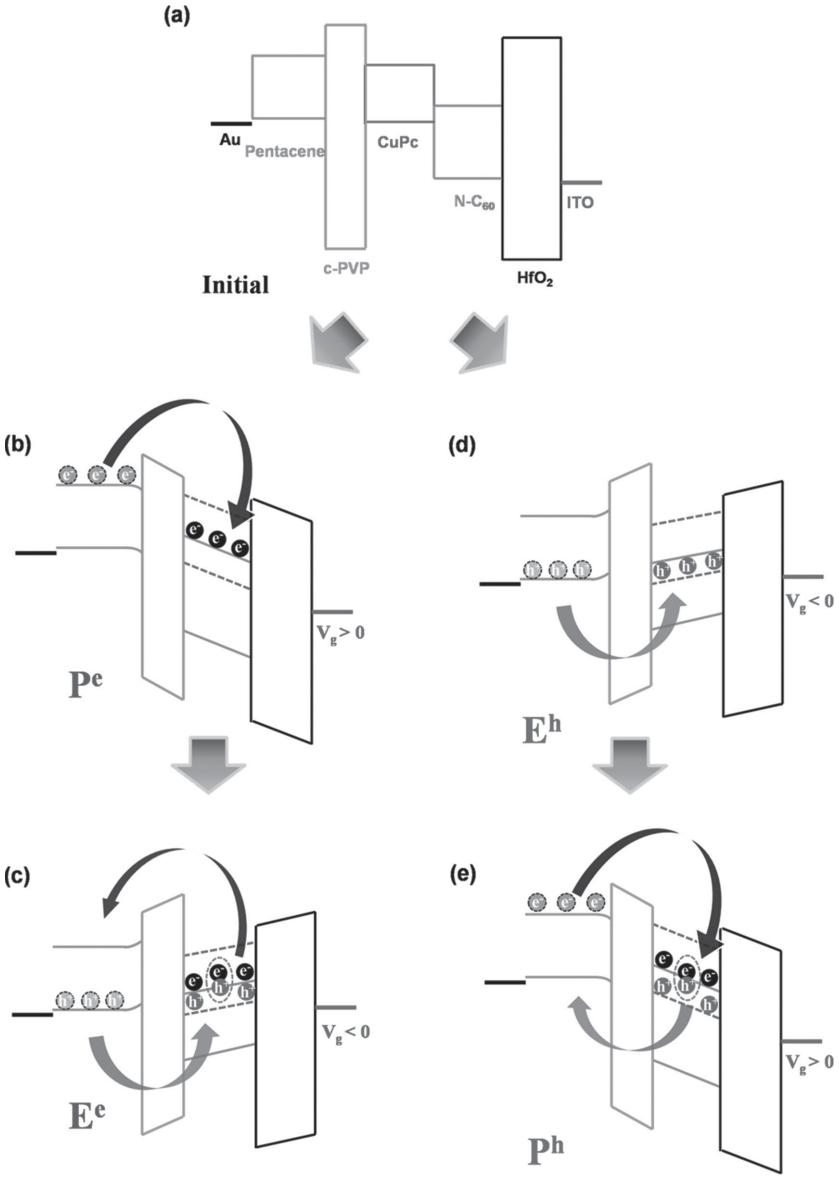


**Figure 5.** Schematic energy band diagram and charge flow of CuPc/N-$C_{60}$-7 double floating-gate memory under programming/erasing operation.

of about 57 and 67 charging holes per CuPc NP. Note that the total numbers of stored charges ($\Delta n^e$ and $\Delta n^h$ for trapped electrons and holes, respectively) are approximately given by:

$$\Delta n = \frac{\Delta V_{th} \times C_i}{e} \quad (1)$$

where $e$ is the elementary charge, $\Delta V_{th}$ the threshold voltage shift, and $C_i$ the specific capacitance for $HfO_2$ dielectric. Two important contributions from here are that, first, the wide memory window in CuPc/N-$C_{60}$-7 double floating-gate devices means the charge capturing ability is enhanced as a result of ambipolar charge trapping, and second, more charge carriers are drawn to N-$C_{60}$ crystals than CuPc NPs, which is attributed to the geometrically high surface-area-to-volume ratio of the needle-shaped $C_{60}$ crystals coupled with good electron transporting/accepting properties.

**Figure 5** summarizes schematically the mechanism that occurs with programming and erasing operations for the double floating-gate OFET memories. In the ambipolar trapping system, the memory properties are achieved by trapping both kinds of charge carriers. Figure 5a shows the proposed flat band diagram of the heterostructured memory devices, which implies that no charge exists in the semiconductor. To balance the positive/negative bias applied to the gate, negative/positive charge carriers are transferred from pentacene to N-$C_{60}$/CuPc by tunneling through the c-PVP layer (corresponding to the programming ($P^h$) process in Figure 5b/erasing ($E^e$) in Figure 5d). Then the trapped charge carriers can migrate out from N-$C_{60}$/CuPc trapping sites or be compensated with the immigrated counter charge carriers transferred from the pentacene to the trapping layer during the following erasing ($E^h$)/programming ($P^e$) process (by applying a reverse voltage pulse in Figure 5c/Figure 5e). As a result, the shifted transfer curves move further back to be close to the initial (I) position (corresponding to erasing ($E^h$) and programming ($P^e$) in Figure 2a). Therefore, threshold voltage can be shifted on both sides by a large enough programming and erasing gate pulse. This indicates that a wide memory window with bidirectional threshold voltage shift is realized through trapped holes in CuPc and electrons in N-$C_{60}$. A well-defined and controllable CuPc/N-$C_{60}$ double floating-gate can be charged or discharged for data levels with good retention and endurance properties. The charge-trapping layer storing the holes/electrons in double storage sites has an ambipolar trapping ability similar to that of the reported single floating-gate.[23,37] Moreover, our present CuPc/N-$C_{60}$ double floating-gate device could precisely control the types of charge trapping carriers and total trapping volumes for high-capacity data storage. Besides, the studied OFET memory devices with easy read-out of threshold voltage shift and a moderately high memory ratio of $10^3$–$10^4$ could exhibit multinary bit programmed states when different gate pulses are applied, further increasing the data storage density.[23,45]

We summarize the advantages of the presented heterostructured CuPc/N-$C_{60}$ double floating-gate organic non-volatile memory as follows: i) multinary bit operation can be performed through double floating-gate layers with ambipolar trapping nature that enlarges the memory window and increases the memory capacity compared to a conventional single floating-gate device, as it creates different transistor characteristics from one OFET memory device. ii) The low-voltage driven OFET memory including a high $k$ dielectric has a low energy consumption and it also has good electrical properties such as mobilities and ON/OFF ratio. iii) Local charge storage in the discrete memory nodes enables more aggressive scaling and tunable trapping density relative to the total charge loss, which is a concern for a continuous planar floating-gate. iv) Good endurance through the direct charging/discharging across the thick-enough tunneling c-PVP dielectric is well characterized.

In conclusion, we have reported a new strategy for fabricating heterostructure double floating-gate memory devices using discrete sub-micrometer-scale N-$C_{60}$ and CuPc NP trapping sites covered by insulating c-PVP. The non-volatile transistor memory characteristics were manipulated by varying the densities/aspect ratios of N-$C_{60}$ and using the double floating-gate device geometry with ambipolar trapping operation to obtain an optimized memory performance. Dual sweeping along the transfer curve confirms that heterostructured CuPc and N-$C_{60}$ double floating-gate has dramatic impacts on the current flow channel of the OFETs. The double floating-gate device can be used as an intensified memory, simultaneously permitting hole and electron trapping in CuPc NPs and N-$C_{60}$, respectively. Wide memory window, low power consumption, high memory density, acceptable retention and endurance properties, and multinary bit memory performance make the fabricated CuPc/N-$C_{60}$-7 double floating-gate non-volatile OFET memory a potential candidate for future advanced non-volatile memory technology.

## Experimental Section

All the commercially available organic compounds were obtained from Aldrich (USA) and used without further purification. Double floating-gate transistor memories were fabricated on ITO glass substrates. $HfO_2$ for the gate dielectric layer was produced by the RF-sputtering method. Then $HfO_2$/ITO substrates were treated with ozone plasma for 5 min. $C_{60}$ single-crystal needles (N-$C_{60}$) obtained by the droplet crystallization method[41] were grown onto a 3-aminopropyl-triethoxysilane (APTES)-modified $HfO_2$/ITO substrate. Subsequently, CuPc was thermally evaporated onto the N-$C_{60}$ layer. Crosslinked poly(4-vinylphenol) (c-PVP) was spin-coated onto the N-$C_{60}$/CuPc double floating-gate as a tunneling layer. 4,4′-(Hexafluoroisopropylidene)diphthalic anhydride (HDA) in propylene glycol monomethyl ether acetate (PGMEA) (20 mg $ml^{-1}$) was used as crosslinking agent and mixed with the base PVP solution (20 mg $ml^{-1}$) as well as 2% of triethylamine (TEA) to promote the esterification reaction and prepare crosslinked c-PVP dielectric thin film. Octadecyltrichlorosilane (ODTS) was used to modify the c-PVP dielectric layer to form a hydrophobic surface. The pentacene semiconducting layer was thermally deposited at a base pressure of $10^{-6}$ Pa. Finally, gold source/drain electrodes (30 nm) were formed by thermal evaporation through a regular shadow mask with a channel length ($L$) and width ($W$) of 50 and 1000 μm, respectively. The electrical characteristics of double floating-gate transistor memories were measured using a Keithley 4200-SCS semiconductor parametric analyzer at room temperature in a $N_2$-filled glove box. At least ten test cells per device were characterized to ensure reproducibility.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

The authors acknowledge financial support from the Ministry of Science and Technology of Taiwan.

Received: August 18, 2014
Published online: October 30, 2014

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