NTU Chem. Eng. Seminar

Moore's Law for Chem. Eng.

摩爾定律

Chia-Hong Jan (簡嘉宏), Chem. Eng./NTU, Taipei, Taiwan (6/2022)

Abstract

Moore's Law has been the guiding principle for the semiconductor industry for more than 60 years. The industry has harvested the 2x transistor/2yrs scaling benefits to fabricated leadership IT products with more computation power, memory bandwidth, energy efficiency and functionality one could have not dreamed. Technology design rules have scaled from 10 um in '70 to low single digit nm now, and soon will be in the Angstrom (Å) scale.

Moore's Law is not a law of "Physics". Instead, it is a law of "Engineering". The secret ingredients of the extension for Moore's Law is to timely integrate the latest and greatest innovations in fundamental science (including Chemical Engineering), device architectures, materials and equipment.

This talk will examine the outlook and roadmap of the key technical areas, including advanced lithography (EUV), disruptive device architectures (GAA and beyond), new materials (2D), and novel 3D packaging solutions (chiplets), to prolong the life of Moore's Law and to let more people harvest the modern marvels of engineering. The speaker will specifically highlight the past and forward-looking technical contributions from the colleagues of Chem. Eng. community.

Long Live the Moore's Law.....

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Chia-Hong Jan

Chia-Hong Jan, Ph. D., MBA

Intel Senior Fellow

Technology and Manufacturing Group, Intel Corp.

IEEE Fellow, IEEE

Dr. Chia-Hong Jan is an Intel executive, holding the title of Intel Senior Fellow and the Technologist of the Technology and Manufacturing Group (TMG). He was the Director of High-Performance Computing (HPC) and System on Chip (SoC) technology integration, and responsible for Intel's advanced logic process technology development used in high-performance and SoC product segments, including data center, cloud server, desktop, laptop, notebook, tablet, smartphone, application-specific integrated circuits, field-programmable gate arrays and wireless communication products.

The Institute of Electrical and Electronics Engineers (IEEE) has named Chia-Hong Jan among its 2017 class of fellows. The honor recognizes Jan for his leadership in developing low power logic technologies for System-on-Chip (SoC).

Since joining Intel in 1991, Jan has held various technical and leadership roles in the Portland Technology Development organization related to the development of 0.8μm, 0.55μm, 0.35μm, 0.25μm, 0.18μm, 0.13μm, 90nm, 65nm, 45nm, 32nm, 22nm, 14nm and 7nm advanced CMOS technologies. He was the group leader for rapid thermal processing and advanced silicon deposition engineering, working on the development of novel salicide technology, advanced gate oxide processes, source and drain junction engineering, and epi SiGe technology for strained silicon. As the manager of 90nm interconnect integration, he led the team credited with being the first in the industry to successfully integrate low-k ILD materials for high-performance microprocessors. He was also the program manager for the 65nm low-power chipset process technology, and for 45nm, 32nm, 22nm and 14 nm SoC process technology for Intel® Atom™ processor–based low-power products, including micro-servers, tablets and smartphones, and chipsets, wireless, RF and FPGA products.

Jan holds more than 120 U.S. patents in the field of semiconductor manufacturing process and integration. He has authored/co-authored more than 40 technical papers related to CMOS processing technology. Jan has received three Intel achievement Awards and was honored with the UW-Madison College of Engineering's Distinguished Achievement Award in 2008.

Jan holds a bachelor's degree in chemical engineering and an MBA degree from National Taiwan University. He also earned a master's degree and Ph.D. in Materials Science from the University of Wisconsin-Madison.

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Chia-Hong Jan on Chem. Eng. News Bulletin 2010

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本系系友簡嘉宏博士獲選英特爾院士(intel fellow)

發佈日期:**2010-04-07**
發佈人:**董觀宇**
相關連結

簡嘉宏博士　畢業於國立台灣大學化學工程學系(1982)，1986年獲國立台灣大學工商管理碩士，分別於1988年與1991年　獲得美國威斯康辛大學麥迪遜校區材料科學碩士與博士學位。目前是英特爾院士，英特爾公司SoC積體電路技術集團的技術和製造部門負責人，為第一位來自國立台灣大學的英特爾院士(intel fellow)。

簡嘉宏博士是英特爾研究員與SoC積體電路技術集團的技術和製造部門負責人。在這個職位上，簡博士管理英特爾公司所有SoC產品的32奈米和22奈米製程技術　，包括超低功耗的移動網絡設備，netbook處理器，消耗性電子產品，嵌入式產品，無線通信應用和 芯片組 /圖形處理器。

簡博士自從　1991年加盟英特爾後，擁有多項技術及身居0.8um，　0.55μm，0.35微米，0.25微米，0.18微米，0.13微米，90奈米，65奈米，45奈米，32奈米波特蘭技術發展(Portland　Technology Development)和現在　22奈米先進的CMOS技術發展的管理職位。他是快速熱的處理(RTP)的和先進的矽沉積(ASD)的小組負責人，　工作目標在發展新型矽化物技術，先進的gate oxide processes，源/漏樞紐工程和磊晶矽鍺 應變矽技術。他帶領的團隊，率先整合　新矽化物材料，包括引入鈦(0.55μm)，　鈷(0.18)和鎳進入basic　logic CMOS處理器。他亦是 90納米交結積體電路部門經理，和他的團隊是第一個 在工業界成功整合low-k ILD材料應用於高功能微處理器者。他同時還是 Intel® Atom™ processor □ased low-power products(英特爾®凌動™處理器二叉樹低功耗產品)中65奈米低功耗芯片製造技術與45奈米SoC製造技術項目經理，此項產品針對有效利用創新的high-k/metal gate技術於SoC領先應用於工業界。

在半導體製程與積體電路領域中，簡博士擁有　37項美國專利 。他已發表超過　40篇與CMOS加工技術有關的技術 論文。獲得3項 英特爾成就獎，並在2008年獲頒威斯康辛大學麥迪遜分校工程學院傑出成就獎。

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