Seminar Introduction

Silicon wafer is the foundation of semiconductor industry. Silicon wafer industry is focusing on fabricating wafers with less defects, flatter and smoother surface, higher mechanical strength, and lower impurity. “Defect Engineering” is the process to engineer silicon wafers to meet special needs of different technology node. Especially, the IC industry is looking for electronic devices to be smarter (faster), smaller (higher capacity per area), lower energy consuming (longer battery lifetime). With the migration of Design rule shrinkage from Micon to Sub-Micron and now to Nano-Meter scale, silicon wafering technology must be developed to meet the requirements. Currently, 10nm design rule is under pilot-production at Intel and TSMC. With such technology advancing, wafer requirement is more and more critical, such as low impurity (Surface Metal <1E9 atoms/cm^2), less surface particles (Surface Particle @37nm <15 count/wafers), super flat local geometry (<20nm height variation within a die), and global geometry (<0.20um within wafer).
Today’s presentation will show you how silicon is made and how to process flat and low impurity silicon wafers as described in below flow.